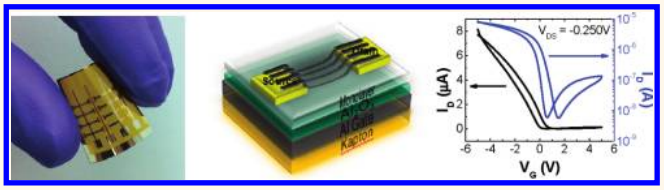
Flexible, Low-Voltage, and Low-Hysteresis PbSe Nanowire Field-Effect Transistors

David K. Kim,[†] Yuming Lai,[‡] Tarun R. Vemulkar,[†] and Cherie R. Kagan[†,‡,§,*]

[†]Department of Materials Science and Engineering, [‡]Department of Electrical and Systems Engineering, and [§]Department of Chemistry, University of Pennsylvania, Philadelphia, Pennsylvania, United States

ABSTRACT



We report low-hysteresis, ambipolar bottom gold contact, colloidal PbSe nanowire (NW) field-effect transistors (FETs) by chemically modifying the silicon dioxide (SiO_2) gate dielectric surface to overcome carrier trapping at the NW-gate dielectric interface. While water bound to silanol groups at the SiO_2 surface are believed to give rise to hysteresis in FETs of a wide range of nanoscale materials, we show that dehydration and silanization are insufficient in reducing PbSe NW FET hysteresis. Encapsulating PbSe NW FETs in cured poly(methyl) methacrylate (PMMA), dehydrates and uniquely passivates the SiO_2 surface, to form low-hysteresis FETs. Annealing predominantly p-type ambipolar PbSe NW FETs switches the FET behavior to predominantly n-type ambipolar, both with and without PMMA passivation. Heating the PbSe NW devices desorbs surface bound oxygen, even present in the atmosphere of an inert glovebox. Upon cooling, overtime oxygen readsorption switches the FET polarity to predominantly p-type ambipolar behavior, but PMMA encapsulation maintains low hysteresis. Unfortunately PMMA is sensitive to most solvents and heat treatments and therefore its application for nanostructured material deposition and doping is limited. Seeking a robust, general platform for low-hysteresis FETs we explored a variety of hydroxyl-free substrate surfaces, including silicon nitride, polyimide, and parylene, which show reduced electron trapping, but still large hysteresis. We identified a robust dielectric stack by assembling octadecylphosphonic acid (ODPA) on aluminum oxide (Al_2O_3) to form low-hysteresis FETs. We further integrated the ODPA/Al_2O_3 gate dielectric stack on flexible substrates to demonstrate low-hysteresis, low-voltage FETs, and the promise of these nanostructured materials in flexible, electronic circuitry.

KEYWORDS: nanocrystals · colloidal nanowires · low-hysteresis · low voltage · flexible transistors

Large hysteresis has been observed in both colloidal PbSe nanowire (NW) and nanocrystal (NC) field-effect transistors (FETs),[1−6] and more broadly in other colloidal semiconductor NW and NC FETs,[7−10] and is currently limiting fundamental studies of charge transport, device performance, and application in more complex, integrated circuits. While it is widely believed that the presence of surface-bound water that hydrogen-bonds to the silanol groups on the silicon dioxide (SiO_2) gate dielectric surface is principally responsible for hysteresis in carbon nanotube (CNT),[11,12] organic,[13,14] ZnO NW,[15] and Si NW FETs,[16,17] hydroxyl passivated and dehydrated PbSe NC[2,3] and NW devices show no significant improvement in the large hysteresis. It has been reported that coating single CNT devices with cured poly(methyl methacrylate) (PMMA) down to the gate dielectric surface nearly eliminates hysteresis.[11,18] This has been attributed to several key factors: (1) curing the PMMA releases surface bound water on both the dielectric and nanotube surfaces that causes hysteresis, (2) the carbonyl groups in PMMA can bond with the silanol groups on SiO_2, and (3) PMMA is hydrophobic, and both factors 2 and 3 keep water from being readsorbed, preventing hysteresis from readily returning.

Here we report a similar reduction in hysteresis for PbSe NW FETs fabricated atop SiO_2 gate dielectric layers thermally grown on a Si back-gate when encapsulated in PMMA, providing a model system to understand more generally how to reduce hysteresis in FETs from colloidal nanostructures. Unlike NC FETs, which are additionally complicated by interparticle spacing and film cracking, which may give rise to trap sites within the semiconductor active layer,[1−3,10] single crystalline colloidal NW FETs are an ideal system to investigate the role of charge transport[19] and the influence of device interfaces on hysteresis. Similar to CNT FETs, we show that the reduced hysteresis in PbSe NW FETs encapsulated in PMMA is consistent with the unique hydrogen bonding that occurs between the hydroxyl terminated surface of the SiO_2 gate dielectric layer and the carbonyl group in PMMA.[11,20,21] PbSe NWs aligned *via* electric field assembly only span approximately 5−10% of the device channel, so PMMA can both encapsulate

* Address correspondence to kagan@seas.upenn.edu.

Received for review October 13, 2011 and accepted November 15, 2011.

Published online November 15, 2011
10.1021/nn203948x

individual NWs and penetrate to the gate dielectric surface to interact with the hydroxyl groups in reducing hysteresis. However since most colloidal NC films deposited by various techniques form uniform and continuous thin films (spincasting,[3,6] dip-coating,[2] and dropcasting[5]), deposition of a top PMMA coating would be ineffective as PMMA would not penetrate to the SiO_2 interface needed to reduce trapping at the semiconductor-dielectric interface. Further, since PMMA cannot withstand the solvents and chemical treatments used in the deposition of many NC materials and in their doping, it is necessary to develop a robust bottom gate dielectric stack that does not require PMMA as a passivating layer.

We report bottom gold contact PbSe FETs atop a range of gate dielectric materials and show hysteresis is consistent with carrier trapping at the NW-gate dielectric surface. Despite heat treatments and the use of hydroxyl-free dielectric layers, large hysteresis is observed on hydrophilic silicon nitride (SiN) and hydrophobic polymer surfaces, indicating that surface water and charge-trapping hydroxyl groups in PbSe NW FETs are not solely responsible for the observed hysteresis. By modifying the gate dielectric surface chemistry we fabricate ambipolar predominantly p and predominantly n-type FETs with dramatically reduced hysteresis. We have identified a surface modified gate dielectric stack, assembling octadecylphosphonic acid (ODPA) on aluminum oxide (Al_2O_3), that allows low-hysteresis FET operation. Further, by implementing this device geometry on flexible substrates, we show low-hysteresis and low-voltage operation on plastics and the promise of integrating these materials in complex integrated circuits.

RESULTS AND DISCUSSION

Encapsulation with Poly(methyl methacrylate) (PMMA). Similar to our previous study,[19] wet-chemically synthesized, straight single crystalline PbSe NWs approximately 10 nm in diameter were aligned under an electric field of 10^4 to 10^5 V/cm between gold source and drain contacts to form FETs. FETs with channel lengths of 20 μm were fabricated atop 250 nm of silicon dioxide thermally grown on highly n-doped silicon wafers, serving as the gate dielectric layer and back-gate of the FETs, respectively. NW FETs were well washed in ethanol and chloroform to remove surface bound ligands, since insufficient cleaning leads to poor current modulation. Devices were then treated with 4.0 M of hydrazine overnight to increase the current levels and reduce contact resistance to become predominantly n-type, and reverted back to predominantly p-type by pulling low vacuum (30 mTorr) for an hour.[19] Posthydrazine treated PbSe NW FETs exhibit both hole and electron transport, but stronger hole transport gives rise to predominantly p-type ambipolar behavior. Rigorous air-free conditions were used from synthesis, purification, characterization, and device fabrication to prevent unintentional oxidation of the NWs, which has been shown to suppress the electron current[1,22,23] and inherent ambipolar[19] behavior in PbSe nanostructures as oxygen creates acceptor states in PbSe, effectively acting as a p-dopant.

PMMA 495 A4 (4 wt % PMMA in anisole from MicroChem) was degassed, brought into the glovebox and 180 nm films were spincast atop predominantly p-type ambipolar PbSe FETs and baked in inert atmosphere at 180 °C for 2 min to cure completely Figure 1A). The drain current (I_D) *versus* gate voltage (V_G) characteristics show that the originally predominantly p-type device with hysteresis of 30 V became a predominantly n-type device with reduced hysteresis of 15 V (Figure 1B and Supporting Information Figure S1A). Device hysteresis is evaluated from the difference in threshold voltage, calculated as the intercept in a linear fit of the I_D-V_G curve, for each sweep direction in V_G. Devices coated with PMMA retained the reduced hysteresis of 15 V over several weeks, but the charge transport characteristics shifted from predominantly n-type back to predominantly p-type over time (Supporting Information, Figure S1B), which is discussed further in the next section. Removal of the PMMA with acetone returned the device to its original p-type behavior with large hysteresis of 30 V, as evidenced by the similar I_D-V_G curves before and after PMMA encapsulation, showing that the effects of PMMA are completely reversible. Subsequent spin-casting, heating, and removal with acetone cycles have been repeatedly performed with independently fabricated devices from multiple synthetic batches of NW solutions and are shown to be consistently reversible and repeatable.

For PbSe NW FETs, the reduction in hysteresis even occurs if the sample were not pretreated in 4.0 M of hydrazine (Supporting Information, Figure S1C), which has been shown to improve the current levels and dope the contact regions at these concentrations,[19] indicating that charge transfer doping of the contact/metal interface is not responsible for hysteresis reduction. To test whether the contacts or bulk were responsible for hysteresis reduction, a 50 nm thick SiO_2 blocking layer was fabricated, with rigorous air-free techniques,[19] on top of 19 μm of the 20 μm channel to selectively encapsulate 0.5 μm of the NW with PMMA at the NW-source and drain interfaces (Figure 1C). The I_D-V_G characteristics show that the hysteresis remains unchanged when selectively encapsulating only the contacts (Figure 1D). Using a different blocking layer length of 18 μm to selectively encapsulate 1.0 μm of the NW at each of the source and drain contacts with PMMA shows a more noticeable reduction in hysteresis (Supporting Information, Figure S1D). The reduction is not as significant as when 100% of the channel was passivated with PMMA, indicating that the semiconductor NW–gate dielectric interface dominates hysteresis in these devices. Measuring devices at lower temperatures also reduced hysteresis (Supporting

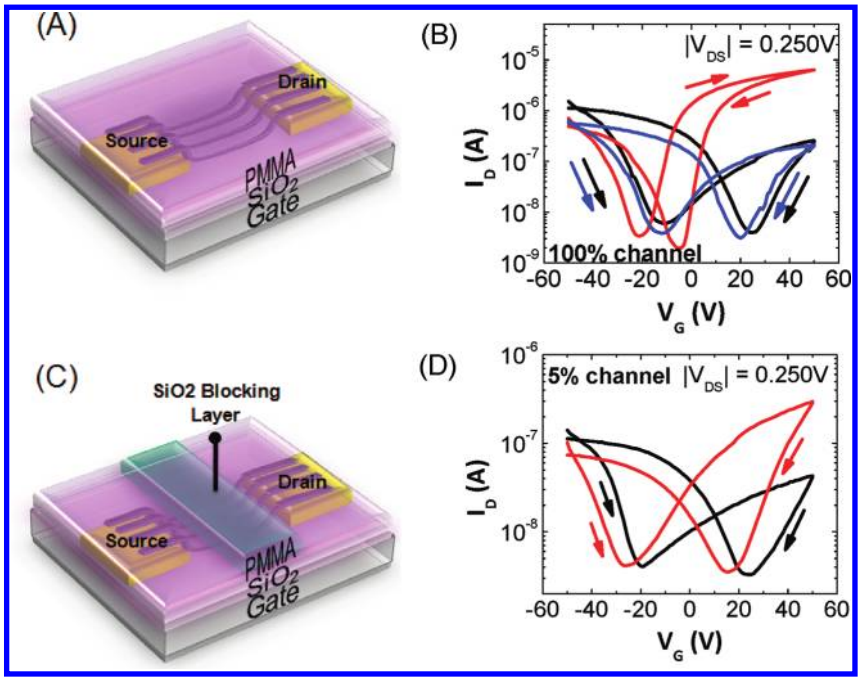


Figure 1. (A) Schematic of a PbSe NW FET with PMMA spincast on top and subsequently cured at 180 °C for 2 min. (B) I_D-V_G characteristics for a PbSe NW FET uncoated (black), with PMMA spincast and cured at 180 °C for two minutes (red) and with PMMA subsequently removed with acetone (blue). (C) Schematic of a PbSe NW FET with a SiO_2 blocking layer covering 95% of the NW channel and PMMA spincast on top and subsequently baked at 180 °C for 2 min. (D) I_D-V_G characteristics of a PbSe NW FET with a SiO_2 blocking layer covering 95% of the NW channel uncoated (black) and with PMMA spincast on top covering the remaining exposed 5% of the channel at the source and drain contact regions and cured at 180 °C for two minutes (red).

Information, Figure S1E) in PbSe NW FETs similar to PbSe NC FETs,[6] suggesting that the observed hysteresis is temperature dependent.

Unlike CNT FETs, which were encapsulated in PMMA in atmosphere, all encapsulations of PbSe FETs had to be done under the inert conditions of the nitrogen-filled glovebox due to the sensitivity of PbSe NWs to oxygen. Even with devices already passivated with PMMA, exposing the NW FETs to atmospheric conditions immediately increased the hysteresis to large values and made the FETs unipolar p-type, losing their electron current and therefore ambipolar behavior (Supporting Information, Figure S1F). Interestingly, upon removal of the PMMA with anhydrous acetone in the glovebox, the devices were returned to their original ambipolar predominantly p-type behavior despite being exposed to atmosphere for 6 h; in contrast exposure of unpassivated NW FETs leads to irreversible oxidation and changes in the FET characteristics. This indicates that PMMA may be a sufficient blocking layer to prevent irreversible oxidation of the NWs, suggesting that short exposure to atmosphere of PMMA coated structures may allow e-beam lithography to provide a good route to fabricate advanced device structures while preserving the intrinsic properties of very oxygen and water sensitive nanomaterials.

The Effect of Oxygen on PbSe NWs. We investigated the polarity switching (from ambipolar predominantly p- to n-type) observed upon encapsulating the PbSe NW FETs in PMMA. We confirmed that PMMA from different sources had no unintentional impurities that could lead to the observed n-type conversion and PMMA of varying molecular weight displayed nearly identical I_D-V_G behavior (Supporting Information, Figure S2). Since the NW FETs are heated during the curing of PMMA, we studied the role of heating and cooling alone on the electrical behavior of the FETs. Without any PMMA encapsulant, heating the original, ambipolar predominantly p-type PbSe FET for 2 min at 180 °C converted the device to ambipolar predominantly n-type behavior. Devices that were heated for 2 min between 50 and 180 °C show a clear transition, with the electron current increasing and the hole current decreasing with increasing annealing temperatures, becoming equally ambipolar around 150 °C and then predominantly n-type at higher temperatures (Figure 2A and Supporting Information, Figure S3A,B), for the same 2 min of annealing. Samples that were heated for 1 h between 100 and 180 °C show a similar trend in both the electron and hole currents, indicating that the polarity switching happens within the first 2 min of heating (Figure 2A and Supporting Information, Figure S3C,D). Twenty-four hours after removing the device from heat, the predominantly n-type character converted back to its original predominantly p-type behavior (Figure 2B and Supporting Information, Figure S3E,F), similar to devices coated in PMMA. Both the log of the electron and hole current levels change linearly over the log of the time. Conversion of the device characteristics upon heating and cooling

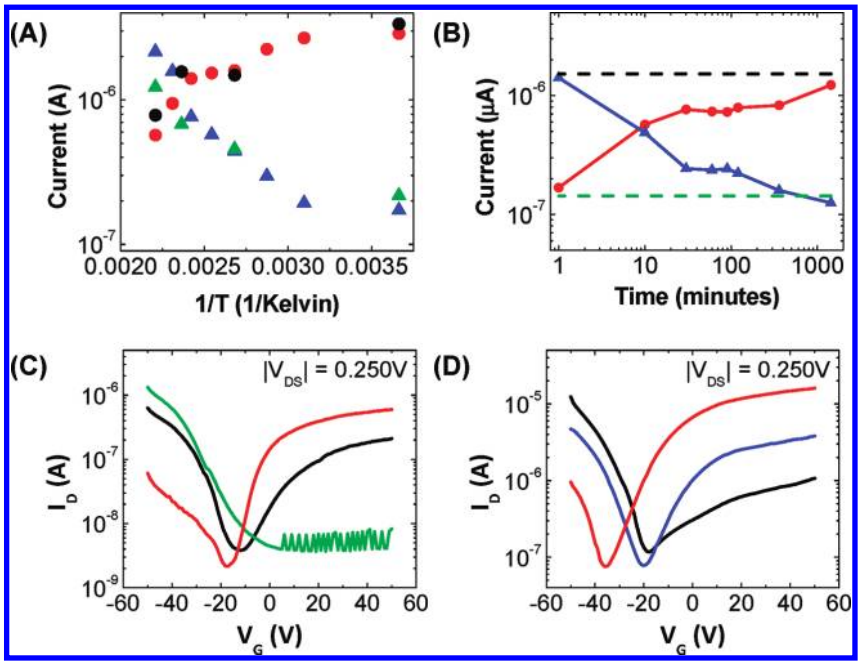


Figure 2. (A) On currents at $|V_G|$ = 50 V for electrons as a function of annealing temperature for 2 min (blue) and 60 min (green), and for holes for 2 min (red) and 60 min (black). (B) Time evolution of electron (blue) and hole (red) on currents over 24 h after cooling, as well as original currents levels before heating for electrons (green dash line) and holes (black dash line). (C) I_D-V_G characteristics of PbSe NW FETs before treatment (black), 10 s UV-ozone exposure (green) and heating at 180 °C for 2 min (red). (D) I_D-V_G characteristics of PbSe NW FETs before vacuum (black), 1 day under vacuum (blue), and 2 days under vacuum (red).

was carried out consecutive times on the same device, and found to yield similar current levels. Similarly, reheating/cooling PMMA coated samples would switch the polarity of the FET behavior.

PbSe is extremely sensitive to oxygen exposure. Even at low-exposure levels of 5.3×10^{-3} Torr (<10 ppm), oxygen has been shown to adsorb on the surface of PbSe nanostructures reversibly to dope it p-type.[1] Therefore, it can be expected that even when storing air-free synthesized PbSe nanostructures inside a nitrogen glovebox, small traces of oxygen are enough to p-dope it over time until the surface is saturated with adsorbed oxygen to favor ambipolar predominantly p-type behavior. This is different from the irreversible exposure at higher oxygen concentrations around 0.87 Torr[1] (>1000 ppm), where oxygen will form covalent bonds with the NW surface and possibly the bulk, and lead to formation of permanent lead−selenide−oxides that suppress electron currents.[24,25] Annealing PbSe NWs in a nitrogen glovebox may provide enough energy to desorb the surface-bound oxygen that is acting as an unintentional p-type dopant. PbSe thin films and crystalline powders have been reported to desorb surface oxygen upon heating in vacuum, giving rise to changes in semiconductor conductivity and type.[26,27] To test whether heat desorbs the oxygen on the surface of PbSe NWs, samples were exposed to UV−ozone for 10 s, which has been demonstrated to intentionally and controllably oxygen-dope PbSe NWs to form unipolar p-type FETs[19] and PbS NC solar cells.[28] Heating the oxidized PbSe NW FET in the glovebox returned the device's electron current (Figure 2C), showing the oxygen-effect to be reversible with heat.

The increase in electron current at the expense of the hole current with increasing temperature (Figure 2A), suggests the Fermi level shifts as the p-doping level is reduced and oxygen is desorbed. Using the changes in electron and hole currents with temperature, assuming an Arrhenius activated energy process,[29] we find an activation energy of *ca.* 0.2−0.3 eV for the desorption of oxygen. Differences in electron and hole trapping and injection may give rise to variations in threshold voltages (Supporting Information, Figure S3A−D) and therefore the calculated activation energies. These results indicate that after oxygen desorption PbSe NW FETs are ambipolar predominantly n-type FETs, which can be attributed to two factors. First, it was reported that exposing PbSe NCs to nitrogen reversibly converts it to n-type,[1] which may contribute to the switch in carrier transport after annealing since the PbSe NW surface is now accessible to nitrogen-doping. Second, PbSe is known to be extremely sensitive to deviations in stoichiometry. Studies of single crystal powders and thin films have shown PbSe with excess lead forms an n-type semiconductor, whereas with excess selenium, forms a p-type semiconductor.[27,30−33] It has been reported in the literature that colloidal PbSe NCs are characterized by an excess of lead on their surface.[34,35] Since NWs are formed through oriented attachment of many colloidal

TABLE 1. Hysteresis for PbSe NW FETs Fabricated with Different Gate Dielectric Stacks on Top of 250 nm Thermally Grown SiO_2 and with Surface-Modified Gate Dielectric Surfaces

	SiO + HMDS (250 nm)	SiN untreated (35 nm)	polyimide (180 nm)	parylene (250 nm)	Al_2O_3 untreated (20 nm)	Al_2O_3 + ODPA (20 nm)
treatment	ΔV_{th} [volts]	ΔV_{th} [volts]	ΔV_{th} [volts]	ΔV_{th} [Volts]	ΔV_{th} [volts]	ΔV_{th} [volts]
aligned and EtOH	41.7 ± 12.7	60.7 ± 7.4	60.9 ± 10.2	32.5 ± 6.7	58.2 ± 5.10	32.1 ± 10.4
24 h after heating	39.4 ± 7.0	41.8 ± 6.2	58.8 ± 10.8	27.6 ± 3.4	38.4 ± 8.14	10.0 ± 7.0
PMMA	15.3 ± 7.5	27.5 ± 2.4	39.4 ± 5.5	33.7 ± 2.4	19.1 ± 1.0	6.6 ± 2.3

PbSe NCs,[36] it is likely that colloidal PbSe NWs may exhibit an excess of lead, favoring predominantly n-type behavior.

Upon removing the NW FETs from heat, over the next 24 h, trace amounts of oxygen reversibly adsorb to the NW surface to return it to predominantly p-type behavior. Since devices were kept in a glovebox with low-oxygen content, it may take considerable time to adsorb enough oxygen to become reversibly p-doped. We estimated in a glovebox with O_2 levels of 0.1 ppm, it would take approximately 20 h to adsorb a monolayer of oxygen, using rates of oxygen uptake at room temperature from early studies of PbSe single crystal powders[37] and accounting for the differences in PbSe surface area and oxygen pressure. This agrees well with both our experiments (Figure 2B) and literature report on oxygen readsorption times of 20−24 h upon cooling for PbSe thin films in vacuum.[26] PbSe NW FETs placed and measured under high vacuum (10^{-7}−10^{-6} Torr) showed a slow conversion to predominantly n-type behavior (Figure 2D), indicating that adsorbed oxygen is slowly desorbed from the PbSe NW surface, similar to ethanedithiol (EDT)-treated PbSe NCs that exhibit ambipolar predominantly n-type transport when measured in vacuum.[1] However, due to the extreme sensitivity of PbSe to oxygen, even inside a nitrogen glovebox, in most cases PbSe nanostructures would preferentially exhibit hole transport.

Modifying the Dielectric Surface to Reduce Hysteresis. It is widely believed that the presence of surface-bound water that hydrogen-bonds to the silanol groups on the SiO_2 gate dielectric surface is principally responsible for hysteresis in CNT,[11,12] organic,[13,14] ZnO NW,[15] and Si NW FETs.[16,17] By encapsulating PbSe NW FETs in PMMA, the baking process to cure the PMMA should desorb the surface bound water and the hydrophobic nature of the PMMA coating would ideally prevent water readsorption. The surface-bound water on SiO_2 is also known to trap electrons,[38,39] which is evident in lower electron currents in FETs of a wide-range of materials. Therefore, eliminating surfaces that are easily hydrated (such as hydroxyl groups) or annealing the PbSe NW FETs should remove the surface bound water and cause a reduction in hysteresis and increase of electron current, even without the use of PMMA. We modified the SiO_2 gate dielectric with two commonly used methods to eliminate the surface adsorbed water.

First, prior to electric field alignment of the NWs, all SiO_2 substrates were treated with hexamethyldisilazane (HMDS) prior to electric field alignment. By passivating the polar silanol groups with trimethylsilyl-terminated groups, the surface exhibits a lower affinity for adsorbed water,[2,3,40] which should reduce the density of charge traps and the hysteresis. However, as reported with PbSe NCs,[2−4] surface modification of SiO_2 with HMDS did not cause a significant reduction in the hysteresis, especially when compared to devices passivated with PMMA [Table 1]. It has also been reported that octadecyltrimethoxysilane (OTMS) treated PbSe NC FETs exhibit large transients at room temperature.[6]

Second, it has been reported that water-bound to silanols on SiO_2 can be removed by heating in dry environments at temperatures of 150 °C or above.[41] More recent studies have suggested that temperatures of 200 °C[11,40] are needed to fully dehydrate the SiO_2 surface, hence devices were also heated under vacuum (<0.1 Torr) for 6 h at 200 °C as a comparison. The extended vacuum 200 °C heat treatment yielded hysteresis values similar to that for devices only heated for 2 min in a glovebox at 180 °C, indicating that the majority of water desorption occurred in the first few minutes of annealing PbSe NW FETs in inert atmosphere. Devices that were measured 24 h after heating exhibited slightly reduced hysteresis and enhanced electron currents, suggesting that dehydration or HMDS passivation are not enough to significantly reduce the large hysteresis (Figure 3A and Table 1). Since SiO_2 surfaces inherently have hydroxyl groups that can be easily saturated with surface-bound water, we replaced the SiO_2 surface with reported hydroxyl-free dielectric surfaces.

Hydroxyl-free hydrophilic SiN,[42,43] and hydrophobic polyimide[44,45] and parylene[39,46] were employed because these surfaces are not hydrated by water molecules that are hydrogen-bonded to silanols as in SiO_2.[40,41] All samples were heated at 180 °C for 2 min to completely remove any residual water after electric field alignment of the NWs, and the FETs were washed with ethanol and chloroform to take away ligands on the surface of the NWs. Measurements were done at least 24 h after heating to allow devices to return to predominantly p-type character. SiN substrates were left unpassivated because silane reagents have poor adhesion to the surface due to the lack of hydroxyl groups and work effectively when untreated.[47] PbSe NW FETs atop SiN (Figure 3B) show higher electron currents and therefore more balanced ambipolar

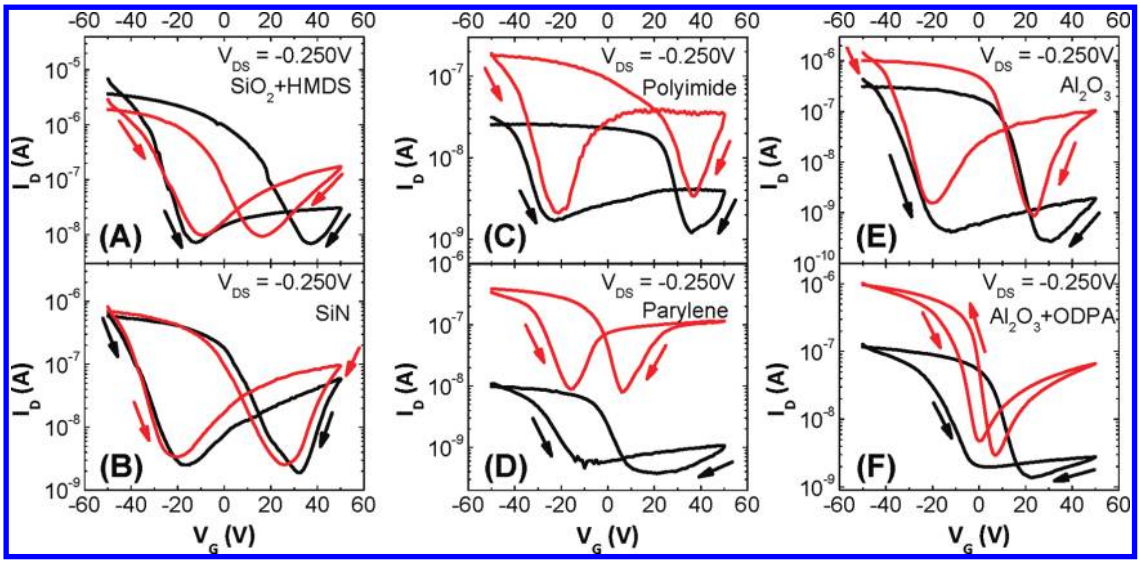


Figure 3. I_D-V_{DS} of PbSe NW FETs fabricated with (A) SiO_2, (B) SiN, (C) polyimide, (D) parylene, (E) Al_2O_3, and (F) octadecylphosphonic acid (ODPA) functionalized Al_2O_3 gate dielectric stacks on top of 250 nm thermally grown SiO_2 before (black) and 24 h after heat treatment at 180 °C for 2 min (red). Note: the current levels in each device differ as the gate dielectric capacitance and number of nanowires spanning the channel are not the same.

behavior, indicative of the lack of hydroxyl groups, especially when compared to HMDS treated SiO_2 (Figure 3A). Despite increased electron currents, the devices still exhibited large hysteresis after annealing. SiN devices were further vacuum heated at 180 °C for several hours to remove any remaining surface-bound water, but did not yield improved hysteresis. Polyimide and parylene are both hydroxyl-free and hydrophobic substrates, which should present ideal surfaces for reduced hysteresis PbSe NW FETs. Heated polyimide and parlylene FETs yielded electron currents more comparable to hole currents (Figure 3C,D) than SiO_2/HMDS FETs, once again indicative of the lack of water-binding hydroxyl groups present on the surface that may act as electron trapping sites. However, while extended vacuum heat treatments at 180 °C and the use of hydroxyl-free, hydrophobic polymer surfaces show enhanced electron currents, the hysteresis remained largely unchanged in these PbSe NW FETs. Further, encapsulating the PbSe NW FETs with PMMA atop the various hydroxyl-free SiN, polyimide, and parylene dielectric surfaces did not yield devices with as low hysteresis as devices fabricated atop SiO_2 gate dielectric surfaces.

While dehydration of the FET and hydroxyl-free dielectric surfaces did not significantly reduce hysteresis, it was suggested that the carbonyl group on PMMA could hydrogen bond to the hydroxyl groups on the SiO_2 surface[20,21,48,49] and aid in hysteresis reduction.[11] FETs with SiO_2 gate dielectrics exhibited the most dramatic reduction in hysteresis when passivated with PMMA, indicating that there is a unique PMMA/SiO_2 surface chemistry that could promote hysteresis reduction in back-gated PbSe NW FETs. Encapsulating PbSe NW FETs with other hydrophobic polymers, such as carbonyl containing polycarbonate and flourinated Cytop (Supporting Information, Figure S3A,B), was not effective in reducing hysteresis, further signifying that PMMA uniquely lowers hysteresis. PMMA is an amphoteric molecule,[50] meaning it can react both as an acid or a base, but has been shown to adsorb more readily to acidic surfaces,[50] so the acidic nature of SiO_2[51−53] will promote PMMA/SiO_2 adsorption. Unfortunately, PMMA devices are sensitive to solvent and heat treatments, and a robust hydroxyl passivation chemistry is necessary for NW and NC device fabrication and doping. Other hydroxyl passivation chemistries were investigated, but PMMA proved to be the most effective encapsulant (Supporting Information, Table S1). In particular, while HMDS is expected to bond with surface SiO_2 hydroxyl groups as well and should exhibit reduced hysteresis, HMDS is sterically hindered and its surface coverage is quite poor, resulting in incomplete passivation of hydroxyl groups,[52,54,55] which is evident in the low-electron currents (Figure 3A). Therefore, we turned our focus to an Al_2O_3 gate dielectric surface because it can be modified with phosphonic acid self-assembled monolayers (SAMs),[56,57] which have been shown to passivate the surface of dielectrics more effectively than silane based SAMs on SiO_2.[57]

Both untreated Al_2O_3 and octadecylphosphonic acid (ODPA) SAM treated Al_2O_3 dielectric layers were used to fabricate electric field aligned PbSe NW FETs, cleaned with solvents to remove ligands and heated at 180 °C for 2 min to remove any remaining solvent. We chose ODPA SAM modification of Al_2O_3 in particular as long alkyl-chain lengths form dense assemblies unlike shorter chain analogues.[58] PbSe NW FETs with bare untreated Al_2O_3 and SiO_2/HMDS gate dielectric layers

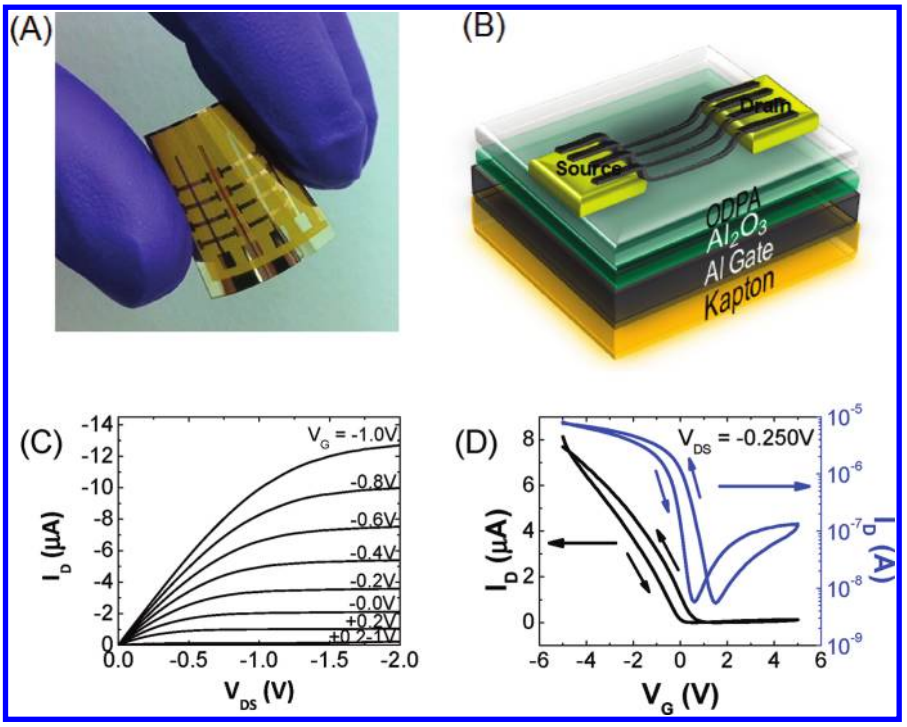


Figure 4. (A) Photograph and (B) schematic of flexible PbSe NW FET on Kapton substrate (C) I_D-V_{DS} and (D) I_D-V_G characteristics showing reduced hysteresis and low-voltage flexible, PbSe NW FET operation.

behaved similarly, displaying low-electron currents, yielding higher electron currents only upon heating (Figure 3A,E). Similar to SiO_2 (even with HMDS passivation), the gate dielectric surface of Al_2O_3 is populated with hydroxyl groups that can act as electron trapping sites to suppress the inherent ambipolar behavior of PbSe NW FETs. PbSe NW FETs atop Al_2O_3 that were encapsulated in PMMA yielded hysteresis values comparable to SiO_2/PMMA devices, since both Al_2O_3 and SiO_2 possess the favorable hydroxyl/PMMA surface chemistry to reduce hysteresis. Treating the basic hydroxyl-terminated surface of Al_2O_3 with acidic ODPA SAMs through acid/base chemistry will form alkyl-(aluminophosphate).[59] PbSe NW FETs fabricated atop Al_2O_3/ODPA yielded devices with hysteresis values even lower than SiO_2/PMMA encapsulated devices (Table 1 and Figure 3F). Unlike the hydrogen bonding that has been reported to occur between SiO_2 hydroxyl groups and the PMMA carbonyl groups, the Al_2O_3/ODPA is a significantly stronger bond that reduces the hysteresis even further. The surface coverage and density of ODPA SAMs on the Al_2O_3 surface is also greater than the silane-based materials on SiO_2.[57] The transistors also retained their low hysteresis when stored in a glovebox for several months, indicating that the Al_2O_3/ODPA is a stable dielectric stack. Devices were also immersed in 4.0 M hydrazine overnight to see if the gate dielectric stack would withstand a commonly used chemical treatment to dope nanostructured materials, become n-type and retain its low hysteresis. While devices became n-type, hydrazine increased the hysteresis significantly by at least 10 V, not only for Al_2O_3/ODPA PbSe NW FETs, but for SiO_2, SiN, and the polymer devices as well (Supporting Information, Table S2). However, when heating post-hydrazine treated transistors at 180 °C for 2 min, devices switched back to ambipolar predominantly p-type behavior and with low hysteresis, indicating that the ODPA treatment could withstand even a caustic base like hydrazine, making it a robust dielectric stack for NW and NC FETs.

Flexible Low-Voltage and Low-Hysteresis FETs. One of the technological benefits of using polyimide, parylene, and Al_2O_3 gate dielectric layers is that these materials can be deposited at low temperatures and integrated in flexible electronics. PbSe NWs were aligned under an electric field on varying dielectric stacks and exhibit ambipolar characteristics similar to devices with SiO_2 on a Si back gate, displaying the versatility of electric-field alignment for a variety of surfaces. Unfortunately, neither polyimide nor parylene are the optimal dielectric materials for low-hysteresis devices. Aluminum oxide has been used as a back gate dielectric material, where Klauk *et al.* showed that flexible ultralow-power organic FETs (OFETs) could be operated using approximately 3−4 nm thicknesses of Al_2O_3.[57] Since electric field alignment requires an electric field of 10^4 to 10^5 V/cm between gold source and drain contacts, 3−4 nm thickness of Al_2O_3 is an insufficient insulator and easily breaks down at such high field strengths, even when passivated with ODPA. An additional 30 nm of ALD (atomic layer deposition) Al_2O_3 was deposited

and passivated with ODPA so electric field alignment could be employed to yield flexible PbSe NW FETs (Figure 4A,B). Devices were heated to remove the solvent as done above to yield low-hysteresis devices. The measured capacitance for the Al_2O_3/ODPA dielectric stack is 0.256 $\pm$ 0.014 $\mu F/cm^2$, allowing for low-voltage operation. Leakage tests were performed on the FETs to verify device behavior was coming from the PbSe NWs (Supporting Information, Figure S5A). Devices still exhibit ambipolar behavior, as evidenced by both the electron and hole transport in I_D-V_{DS} characteristics in both the hole (Figure 4C) and electron accumulation regimes (Supporting Information, Figure S5B) and in I_D-V_G curves (Figure 4D). These are the first flexible, low-voltage (<5 V) and low-hysteresis (<1 V) PbSe NW FETs and show the promise of these nanostructured materials in flexible electronics.

CONCLUSIONS

In summary, we show that surface-bound water is not solely responsible for the observed hysteresis in bottom contact PbSe NW FETs. By encapsulating PbSe NW FETs in PMMA, we fabricated ambipolar predominantly p and predominantly n-type FETs with dramatically reduced hysteresis. Predominantly ambipolar n-type devices could be achieved by annealing or placing devices under high vacuum to desorb the surface bound oxygen, which has been shown to suppress the electron current in PbSe nanostructures. Despite careful air-free handling of the NWs, PbSe exhibits extremely high sensitivity to trace amounts of oxygen, even in an inert glovebox environment. We demonstrated the versatility of electric field alignment by fabricating bottom gold contact PbSe NW FETs atop a range of hydroxyl-free and hydrophobic gate dielectric materials that show enhanced electron currents, but still exhibit large hysteresis. We have identified a surface modified gate dielectric stack, ODPA SAMs on Al_2O_3, that exhibits low-hysteresis FET operation. Exploration of alternative combinations of gate dielectric layers and SAM chemistries and/or surface modification of the NWs themselves may allow the small, residual hysteresis to be eliminated. This robust, low-hysteresis dielectric stack will not only allow us to study the fundamentals of charge transport in PbSe NWs, but in other colloidal nanostructured systems as well. Additionally, by implementing this device geometry on flexible substrates, we show low-hysteresis and low-voltage operation on plastics and the promise of integrating these materials in complex integrated circuits.

METHODS SECTION

Materials for Nanowire Synthesis. All manipulations were carried out using standard Schlenk-line techniques under dry nitrogen. Tri-*n*-octylphosphine (further referred to as TOP, Aldrich, 90%), oleic acid (OA, Aldrich, 90%), diphenyl ether (Aldrich, 99%), amorphous selenium pellets (Aldrich, 99.999%), lead acetate trihydrate (Fisher Scientific Co.), and *n*-tetradecylphosphonic acid (TDPA, Strem, 97%) were used as purchased without further purification. Anhydrous chloroform and hexane were bought from Aldrich. To prepare a 0.167 M stock solution of trioctylphosphine selenide (TOPSe), 1.32 g of selenium was dissolved in 100 mL of TOP overnight by stirring.

Synthesis and Nanowire Alignment Preparation. The PbSe NWs were synthesized according to previously reported methods.[36] Lead acetate trihydrate (0.76 g) was dissolved in 2 mL of OA and 10 mL of diphenyl ether. The solution was heated to 150 °C for 30 min under nitrogen flow in order to form a lead−oleate complex. The solution was then cooled to 60 °C and 4 mL of 0.167 M TOPSe solution was added slowly to prevent premature nucleation of PbSe. The combined lead−oleate/TOPSe solution was injected under vigorous stirring into a hot (250 °C) growth solution containing 0.2 g TDPA dissolved in 15 mL of diphenyl ether. After ~50 s of heating, the reaction mixture was cooled to room temperature using a water bath. Once cooled, the reaction vessel (still under N_2) was transferred to a glovebox, where the crude solution was mixed with equal amounts of hexane, and the nanowires (NWs) were isolated by centrifugation at 4300 rpm for 5 min. All purification was carried out in nitrogen atmosphere using anhydrous solvents. Purified PbSe NW stock solutions were dispersed in octane/nonane at a 1:1 (vol/vol) ratio with several drops of 10 wt % solution hexadecane-graft-polyvinylprrolidone (HD-PVP) copolymer (M_n = ~7300) to improve the dispersibility of the NWs.

Dielectric Preparation. All devices with varying dielectric surfaces, except the flexible device, were fabricated on an n-doped Si wafer with 250 nm thermally grown SiO_2 from Silicon Inc. The Si wafers were treated with UV-ozone for 30 min before deposition of varying dielectrics. All film thicknesses were confirmed using either a capacitance measurement (metal/dielectric/metal) using a HP 4276 A LCZ meter and/or surface profilometer (Tencor, Alpha Step 200). The dielectric constant was assumed to be 3.05 for polyimide, 3.15 for parylene-C, 7.5 for SiN, and 9.0 for Al_2O_3.

Polyimide Dielectric. Polyimide precursors (PI-2611 series) were purchased from HD MicroSystems, and diluted in *N*-methyl-2-pyrrolidone to a ratio of 1:2. The diluted polyimide precursor was then spin coated (3000 rpm for 30 s) and cured (350 °C for 30 min) to form approximately 180 nm polyimide layer.

Parylene Dielectric. Parylene-C was purchased from Specialty Coating Systems and deposited in a PDS 2010 system to a thickness of about 250 nm.

Silicon Nitride. An Oxford Instruments PlasmaLab 100 system was used to deposit 35 nm of plasma-enhanced chemical vapor deposited (PECVD) SiN.

Aluminum Oxide. A Cambridge Nanotech Savannah 200 system was used to deposit 20 nm of atomic layer deposited (ALD) Al_2O_3 at 250 °C using trimethylaluminum and water precursors.

Flexible Device. Kapton 200 Type E films were obtained from DuPont and served as the substrate. Kapton films were cleaned for 5 min each in an ultrasonic bath of ethanol and distilled-H_2O, followed by a 30 min UV-ozone. Using a shadow mask, 20 nm of aluminum was deposited through a shadow mask and then placed in an Oxford Instruments 80Plus parallel-plate reactive ion etcher (RIE). The back-gate sample was briefly exposed to an oxygen plasma (150 W, 15 s) to increase the thickness of the native Al_2O_3 and create hydroxyl groups necessary for ALD Al_2O_3. After forming a thin oxide on the aluminum back-gate, the flexible sample was placed in the Cambridge Nanotech Savannah 200 ALD tool to deposit 30 nm of Al_2O_3.

Device Fabrication. For SiO_2, SiN, and Al_2O_3 dielectric devices, electrodes were patterned using photolithography with a bilayer of Lift-off Resist (LOR3A from MicroChem) and S1813 (Microposit). Samples were photolithographically patterned to define channel lengths of 20 μm and widths of 200 μm using a Karl Suss Mask aligner and developed in MF-319 (Microposit). The exposed sample was cleaned by an oxygen plasma (100W, 3 min) and metal was deposited by e-beam evaporation of 2 nm of Ti and 18 nm Au. Metal was subsequently lifted off using Remover PG (MicroChem). The SiO_2 fabricated devices were then put in a YES (Yield Engineering Systems) Oven, where the fabricated devices were first cleaned with an O_2 plasma and then vapor primed with hexamethyldisilazane (HMDS, Aldrich, 99.9%) for 5 min at 150 °C. The SiN devices were untreated. The Al_2O_3 device was prepared with a self-assembled monolayer following a previously reported procedure.[57] Al_2O_3 devices were submerged in 0.005 M octadecylphosphonic acid (ODPA) (PCI Synthesis) in isopropyl alcohol solution over 16 h to treat the Al_2O_3 surface. Polyimide, parylene and flexible devices were fabricated by evaporating Au through a shadow mask made of silicon nitride membranes with very fine channel lengths of 20 μm and widths of 1260 μm. Flexible devices were similarly treated with ODPA to passivate the Al_2O_3 back-gate.

Nanowire Alignment. NWs were aligned across device structure having a channel length of 20 μm and channel width of 200 μm (SiO_2, SiN and Al_2O_3 dielectric stacks) or channel length of 20 μm and channel width of 1260 μm (Polyimide, Parylene dielectric stacks, Flexible FET). NW solutions were dropcast under dc electric fields of 10^4 to 10^5 V/cm, aligning NW arrays across the prefabricated bottom electrodes. The number of NWs spanning the FET channel is controlled by varying the concentration and volume of the NW solution that is dropcast. The NWs were washed with ethanol and then chloroform to remove the HD-PVP polymer and organics. For n-type conversion of the p-type NW FETs, 4 M of hydrazine (Aldrich, 98%) in acetonitrile (Aldrich, anhydrous, 99.8%) was used **(NOTE: hydrazine is toxic by vapor inhalation and skin absorption)** or heated at 180 °C on a hot plate in nitrogen atmosphere (Torrey Pines). Electric-field directed assembly was carried out in an MBraun nitrogen glovebox and all solvents used were distilled and anhydrous.

An Agilent 4156C parameter analyzer in combination with a Karl Suss PM5 probe station mounted in the nitrogen glovebox was used to measure device characteristics. The source was grounded and a highly n-doped silicon wafer was used as a back gate electrode.

PMMA Encapsulation. PMMA 495 A4 (4 wt % PMMA in anisole from MicroChem) was degassed and brought inside an MBraun nitrogen glovebox. The PMMA was spin coated (3000 rpm for 45 s) and baked under nitrogen at 180 °C for 2 min to form a 180 nm thin film. PMMA ($M_w \approx$ 996K) and anhydrous anisole were also purchased from Aldrich, and combined to make a 4 wt % solution. The PMMA in anisole from Aldrich was also spincast and baked under similar conditions.

Blocking Layer Fabrication. An 50 nm thick SiO_2 blocking layer was fabricated according to previously reported methods.[19] All e-beam resists and developers were degassed and used inside an MBraun nitrogen glovebox. An e-beam resist bilayer of 495 PMMA A4 (MicroChem) and 950 PMMA A4 (Microposit) was spincast and baked under nitrogen at 180 °C for 2 min for each layer. The PMMA coated device was secured in a jar under nitrogen in the glovebox and taken to the e-beam lithography tool, where the blocking layer was exposed. After exposure, the sample was developed in the glovebox with methyl isobutyl ketone in isopropyl alcohol (MIBK/IPA 1:3, Honeywell Burdick and Jackson). E-beam evaporation of the 50 nm SiO_2 blocking layer was carried out in a nitrogen glovebox with an integrated evaporator, followed by lift-off with anhydrous acetone.

Acknowledgment. The authors thank A. Afzali for advice and helpful discussions. D.K.K., T.R.V., Y.L., and C.R.K. acknowledge support from the NSF (NSF DMR-0805155).

Supporting Information Available: Detailed and extended surface treatments and I_D-V_{DS} curves of PbSe NW FETs. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Leschkies, K. S.; Kang, M. S.; Aydil, E. S.; Norris, D. J. Influence of Atmospheric Gases on the Electrical Properties of PbSe Quantum-Dot Films. *J. Phys. Chem. C* **2010**, *114*, 9988–9996.
2. Luther, J. M.; Law, M.; Song, Q.; Perkins, C. L.; Beard, M. C.; Nozik, A. J. Structural, Optical, and Electrical Properties of Self-Assembled Films of PbSe Nanocrystals Treated with 1,2-Ethanedithiol. *ACS Nano* **2008**, *2*, 271–280.
3. Law, M.; Luther, J. M.; Song, Q.; Hughes, B. K.; Perkins, C. L.; Nozik, A. J. Structural, Optical, and Electrical Properties of PbSe Nanocrystal Solids Treated Thermally or with Simple Amines. *J. Am. Chem. Soc.* **2008**, *130*, 5974–5985.
4. Liu, Y.; Gibbs, M.; Puthussery, J.; Gaik, S.; Ihly, R.; Hillhouse, H. W.; Law, M. Dependence of Carrier Mobility on Nanocrystal Size and Ligand Length in PbSe Nanocrystal Solids. *Nano Lett.* **2010**, *10*, 1960–1969.
5. Talapin, D. V.; Murray, C. B. PbSe Nanocrystal Solids for n- and p-channel Thin Film Field-Effect Transistors. *Science* **2005**, *310*, 86–89.
6. Kang, M. S.; Sahu, A.; Norris, D. J.; Frisbie, C. D. Size- and Temperature-Dependent Charge Transport in PbSe Nanocrystal Thin Films. *Nano Lett.* **2011**, *11*, 3887–3892.
7. Lee, J.-S.; Shevchenko, E. V.; Talapin, D. V. Au−PbS Core−-Shell Nanocrystals: Plasmonic Absorption Enhancement and Electrical Doping *via* Intra-particle Charge Transfer. *J. Am. Chem. Soc.* **2008**, *130*, 9673–9675.
8. Seon, J.-B.; Lee, S.; Kim, J.; Jeong, H.-D. Spin-Coated CdS Thin Films for n-Channel Thin Film Transistors. *Chem. Mater.* **2009**, *21*, 604–611.
9. Holman, Z. C.; Liu, C.-Y.; Kortshagen, U. R. Germanium and Silicon Nanocrystal Thin-Film Field-Effect Transistors from Solution. *Nano Lett.* **2010**, *10*, 2661–2666.
10. Talapin, D. V.; Lee, J.-S.; Kovalenko, M. V.; Shevchenko, E. V. Prospects of Colloidal Nanocrystals for Electronic and Optoelectronic Applications. *Chem. Rev.* **2010**, *110*, 389–458.
11. Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y.; Dai, H. Hysteresis Caused by Water Molecules in C9arbon Nanotube Field-Effect Transistors. *Nano Lett.* **2003**, *3*, 193–198.
12. Vosgueritchian, M.; LeMieux, M. C.; Dodge, D.; Bao, Z. Effect of Surface Chemistry on Electronic Properties of Carbon Nanotube Network Thin Film Transistors. *ACS Nano* **2010**, *4*, 6137–6145.
13. Egginger, M.; Bauer, S.; Schwödiauer, R.; Neugebauer, H.; Sariciftci, N. S. Current *versus* Gate Voltage Hysteresis in Organic Field Effect Transistors. *Monatsh. Chem.* **2009**, *140*, 735–750.
14. Gu, G.; Kane, M. G. Moisture Induced Electron Traps and Hysteresis in Pentacene-Based Organic Thin-Film Transistors. *Appl. Phys. Lett.* **2008**, *92*, 053305.
15. Goldberger, J.; Sirbuly, D. J.; Law, M.; Yang, P. ZnO Nanowire Transistors. *J. Phys. Chem. B* **2005**, *109*, 9–14.
16. Wang, D.; Sheriff, B. A.; Heath, J. R. Silicon p-FETs from Ultrahigh Density Nanowire Arrays. *Nano Lett.* **2006**, *6*, 1096–1100.
17. Paska, Y.; Stelzner, T.; Christiansen, S.; Haick, H. Enhanced Sensing of Nonpolar Volatile Organic Compounds by Silicon Nanowire Field Effect Transistors. *ACS Nano* **2011**, *5*, 5620–5626.
18. Ai, N. Walden-newman, W. Song, Q. Kalliakos, S.; Strauf, S. Suppression of Blinking and Enhanced Exciton Emission from Individual Carbon Nanotubes. *ACS Nano* **2011**.
19. Kim, D. K.; Vemulkar, T. R.; Oh, S. J.; Koh, W.-K.; Murray, C. B.; Kagan, C. R. Ambipolar and Unipolar PbSe Nanowire Field-Effect Transistors. *ACS Nano* **2011**, *5*, 3230–3236.
20. Berquier, J.-M.; Arribart, H. Attenuated Total Reflection Fourier Transform Infrared Spectroscopy Study of Poly(methyl methacrylate) Adsorption on a Silica Thin Film: Polymer/Surface Interactions. *Langmuir* **1998**, *14*, 3716–3719.

21. Jia, X.; McCarthy, T. J. Buried Interface Modification Using Supercritical Carbon Dioxide. *Langmuir* **2002**, *18*, 683–687.
22. Rogacheva, E. I.; Tavrina, T. V.; Nashchekina, O. N.; Grigorov, S. N.; Sipatov, A. Y.; Volobuev, V. V.; Dresselhaus, M. S.; Dresselhaus, G. Influence of Oxidation on the Transport Properties of IV−VI-Thin Films. *Physica E* **2003**, *17*, 310–312.
23. Rogacheva, E. I.; Tavrina, T. V.; Grigorov, S. N.; Nashchekina, O. N.; Volobuev, V. V.; Fedorov, A. G.; Nasedkin, K. A.; Dresselhaus, M. S. Effect of Oxidation on the Thermoelectric Properties of PbSe Thin Films. *J. Electron. Mat.* **2002**, *31*, 298–303.
24. Tomaev, V. V.; Makarov, L. L.; Tikhonov, P. A.; Solomennikov, A. A. Oxidation Kinetics of Lead Selenide. *Glass Phys. Chem* **2004**, *30*, 349–355.
25. Popov, V. P.; Tikhonov, P. A.; Tomaev, V. V. Investigation into the Mechanism of Oxidation on the Surface of Lead Selenide Semiconductor Structures. *Glass Phys. Chem.* **2003**, *29*, 494–500.
26. Das, V. D.; Bhat, K. S. Electrical Conductivity of Air-Exposed and Unexposed Lead Selenide Thin Films: Temperature and Size Effects. *Phys. Rev. B* **1989**, *40*, 7696–7703.
27. Bhat, K. S.; Das, V. D. Electrical-Conductivity Changes in PbTe and PbSe Films on Exposure to the Atmosphere. *Phys. Rev. B* **1985**, *32*, 6713–6719.
28. Zhao, N.; Osedach, T. P.; Chang, L.-Y.; Geyer, S. M.; Wanger, D.; Binda, M. T.; Arango, A. C.; Bawendi, M. G.; Bulovic, V. Colloidal PbS quantum Dot Solar Cells with High Fill Factor. *ACS Nano* **2010**, *4*, 3743–3752.
29. Jones, R. The Effect of Oxygen on an Evaporated PbSe Layer. *Proc. Phys. Soc. London, Sect. B* **1957**, *70*, 704–708.
30. Brebrick, R. F.; Gubner, E. PbSe Composition Stability Limits. *Chem. Phys.* **1961**, *36*, 170–172.
31. Dalven, R. A Review of the Semiconductor Properties of PbTe, PbSe, PbS and PbO. *Infrared Phys.* **1969**, *9*, 141–184.
32. Humphrey, J. N.; Scanlon, W. W. Photoconductivity in Lead Selenide. Experimental. *Phys. Rev.* **1957**, *105*, 469–476.
33. Schlichting, U.; Gobrecht, K. The Mobility of Free Carriers in PbSe Crystals. *J. Phys. Chem. Solids* **1973**, *34*, 753–758.
34. Moreels, I.; Lambert, K.; Muynck, D.; De; Vanhaecke, F.; Poelman, D.; Martins, J. C.; Allan, G.; Hens, Z. Composition and Size-Dependent Extinction Coefficient of Colloidal PbSe Quantum Dots. *Chem. Mater.* **2007**, *19*, 6101–6106.
35. Moreels, I.; Fritzinger, B.; Martins, J. C.; Hens, Z. Surface Chemistry of Colloidal PbSe Nanocrystals. *J. Am. Chem. Soc.* **2008**, *130*, 15081–15086.
36. Cho, K.-S.; Talapin, D. V.; Gaschler, W.; Murray, C. B. Designing PbSe Nanowires and Nanorings through Oriented Attachment of Nanoparticles. *J. Am. Chem. Soc.* **2005**, *127*, 7140–7147.
37. Jones, R. H. The Reaction of Oxygen with Lead Selenide. *Proc. Phys. Soc. London, Sect. B* **1957**, *70*, 1025–1032.
38. Saudari, S. R.; Frail, P. R.; Kagan, C. R. Ambipolar transport in solution-deposited pentacene transistors enhanced by molecular engineering of device contacts. *Appl. Phys. Lett.* **2009**, *95*, 023301.
39. Aguirre, C. M.; Levesque, P. L.; Paillet, M.; Lapointe, F.; St-Antoine, B. C.; Desjardins, P.; Martel, R. The Role of the Oxygen/Water Redox Couple in Suppressing Electron Conduction in Field-Effect Transistors. *Adv. Mater.* **2009**, *21*, 3087–3091.
40. Zhuravlev, L. T. The Surface Chemistry of Amorphous Silica. Zhuravlev Model. *Colloid Surf. A* **2000**, *173*, 1–38.
41. Iler, R. K. *The Chemistry of Silica: Solubility, Polymerization, Colloid and Surface Properties, and Biochemistry*; Wiley: New York, 1979.
42. Li, F. M.; Nathan, A.; Wu, Y.; Ong, B. S. Organic Thin-Film Transistor Integration Using Silicon Nitride Gate Dielectric. *Appl. Phys. Lett.* **2007**, *90*, 133514.
43. Li, F. M.; Nathan, A.; Wu, Y.; Ong, B. S. A Comparative Study of Plasma-Enhanced Chemical Vapor Gate Dielectrics for Solution-Processed Polymer Thin-Film Transistor Circuit Integration. *J. Appl. Phys.* **2008**, *104*, 124504.
44. Ahn, T.; Kim, J. W.; Choi, Y.; Yi, M. H. Hybridization of a Low-Temperature Processable Polyimide Gate Insulator for High Performance Pentacene Thin-Film Transistors. *Org. Electron.* **2008**, *9*, 711–720.
45. Kim, J. Y.; Yi, M. H.; Ahn, T. Excellent Heat Resistance Polymeric Gate Insulator for Thin-Film Transistor by Low Temperature and Solution Processing. *Thin Solid Films* **2010**, *518*, 6280–6284.
46. Saudari, S. R.; Lin, Y. J.; Lai, Y.; Kagan, C. R. Device Configurations for Ambipolar Transport in Flexible, Pentacene Transistors. *Adv. Mater.* **2010**, *22*, 5063–5068.
47. Li, F. M.; Dhagat, P.; Haverinen, H. M.; McCulloch, I.; Heeney, M.; Jabbour, G. E.; Nathan, A. Polymer Thin Film Transistor Without Surface Pretreatment on Silicon Nitride Gate Dielectric. *Appl. Phys. Lett.* **2008**, *93*, 073305.
48. Hamieh, T.; Schultz, J. New Approach to Characterise Physicochemical Properties of Solid Substrates by Inverse Gas Chromatography at Infinite Dilution. II. Study of the Transition Temperatures of Poly(methyl methacrylate) at Various Tacticities and of Poly(methyl methacrylate) A. *J. Chromatogr. A* **2002**, *969*, 27–36.
49. Hu, Y. Viscoelastic Properties and Thermal Degradation Kinetics of Silica/PMMA Nanocomposites. *Polym. Degrad. Stab.* **2004**, *84*, 545–553.
50. Papirer, E.; Perrin, J. M.; Siffert, B.; Philipponneau, G. Surface Characteristics of Aluminas in Relation with Polymer Adsorption. *J. Colloid Interface Sci.* **1991**, *144*, 263–270.
51. Kosmulski, M.; Maczka, E.; Rosenholm, J. B. Isoelectric Points of Metal Oxides at High Ionic Strengths. *J. Phys. Chem. B* **2002**, *106*, 2918–2921.
52. Chua, L. L.; Zaumseil, J.; Chang, J. F.; Ou, E. C. W.; Ho, P. K. H.; Sirringhaus, H.; Friend, R. H. General Observation of n-type Field-Effect Behaviour in Organic Semiconductors. *Nature* **2005**, *434*, 194–199.
53. Lewis, J. A. Colloidal Processing of Ceramics. *J. Am. Ceram. Soc.* **2000**, *83*, 2341–2359.
54. Haukka, S.; Roots, A. The Reaction of Hexamethyldisilazane and Subsequent Oxidation of Trimethylsilyl Groups on Silica Studied. *J. Phys. Chem.* **1994**, *98*, 1695–1703.
55. Sindorf, D. W.; Maciel, G. E. Cross-Polarization/Magic-Angle-Spinning Silicon-29 Nuclear Magnetic Resonance Study of Silica Gel Using Trimethylsilane Bonding as a Probe. *J. Phys. Chem.* **1982**, *86*, 5208–5219.
56. Folkers, J. P.; Gorman, C. B.; Laibinis, P. E.; Buchholz, S.; Whitesides, G. M.; Nuzzo, R. G. Self-Assembled Monolayers of Long-Chain Hydroxamic Acids on the Native Oxide of Metals. *Langmuir* **1995**, *11*, 813–824.
57. Klauk, H.; Zschieschang, U.; Pflaum, J.; Halik, M. Ultralow-Power Organic Complementary Circuits. *Nature* **2007**, *445*, 745–748.
58. Spori, D. M.; Venkataraman, N. V.; Tosatti, S. G. P.; Durmaz, F.; Spencer, N. D.; Zürcher, S. Influence of Alkyl Chain Length on Phosphate Self-Assembled Monolayers. *Langmuir* **2007**, *23*, 8053–8060.
59. Goetting, L. B.; Deng, T.; Whitesides, G. M. Microcontact Printing of Alkanephosphonic Acids on Aluminum: Pattern Transfer by Wet Chemical Etching. *Langmuir* **1999**, *15*, 1182–1191.